



Group - A (Short Answer Questions)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
UNIT-I DIGITAL SYSTEMS			
1	Write short notes on binary number systems?	Understand	1
2	Discuss 1's and 2's complement methods of subtraction?	Understand	1
3	Discuss octal number system?	Understand	1
4	State and prove transposition theorem?	Knowledge	1
5	Explain how do you convert AOI logic to NAND logic?	Understand	2
6	Write a short note on five bit BCD codes?	Understand	2
7	Explain the specialty of unit –distance code? State where they are used?	Understand	2
8	Write a short note on error correcting codes?	Understand	2
9	State and prove De-Morgan theorem?	Knowledge	3
10	Discuss what a logic design is and what do u mean by positive logic system?	Understand	2
11	Convert (4085) ₉ into base-5?	Understand	1
12	Write the first 20 decimal digits in base 3?	Understand	1
13	Write the steps involved in unsigned binary subtraction using complements with examples?	Understand	2
14	Explain the addition of two signed binary number along with examples?	Understand	2
15	Differentiate between binary code and BCD code?	Understand	3
16	Explain how binary values are stored in memory?	Understand	2
17	Write the Axiomatic Definitions of Boolean Algebra?	Understand	3

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18	Write a table stating all the postulates and theorems of Boolean Algebra that are required for logic minimization?	Understand	3															
19	Convert $f(x) = x + y'z$ into canonical form?	Understand	3															
20	State and prove idempotent laws of Boolean algebra?	Knowledge	3															
UNIT-II																		
GATE LEVEL MINIMIZATION AND COMBINATION CIRCUITS																		
1	Define K-map? Name its advantages and disadvantages?	Knowledge	5															
2	Write the block diagram of 2-4 and 3-8 decoders?	Understand	8															
3	Define magnitude comparator?	Knowledge	5															
4	Describe what do you mean by look-ahead carry?	Understand	5															
5	Summarize the Boolean function $x'yz + x'yz' + xy'z' + xy'z$ using K-map?	Understand	4															
6	Explain how combinatorial circuits differ from sequential circuits?	Understand	5															
7	Explain what are the IC components used to design combinatorial circuits with MSI and LSI?	Understand	5															
8	Design the two graphic symbols for NAND gate?	Understand	6															
9	Design the two graphic symbols for NOR gate?	Understand	6															
10	Summarize the Boolean function $x'yz + x'yz' + xy'z' + xy'z$ without using K-map?	Understand	4															
11	Explain the properties of EX-OR gate?	Understand	6															
12	Solve the function of fig with AND-OR INVERT implementations? <div style="text-align: center; margin: 10px 0;"> <table border="1" style="border-collapse: collapse;"> <tr> <td style="padding: 2px 5px;">A \ BC</td> <td style="padding: 2px 5px;">00</td> <td style="padding: 2px 5px;">01</td> <td style="padding: 2px 5px;">11</td> <td style="padding: 2px 5px;">10</td> </tr> <tr> <td style="padding: 2px 5px;">0</td> <td style="padding: 2px 5px; text-align: center;">1</td> <td style="padding: 2px 5px; text-align: center;">0</td> <td style="padding: 2px 5px; text-align: center;">0</td> <td style="padding: 2px 5px; text-align: center;">0</td> </tr> <tr> <td style="padding: 2px 5px;">1</td> <td style="padding: 2px 5px; text-align: center;">0</td> <td style="padding: 2px 5px; text-align: center;">0</td> <td style="padding: 2px 5px; text-align: center;">0</td> <td style="padding: 2px 5px; text-align: center;">1</td> </tr> </table> </div>	A \ BC	00	01	11	10	0	1	0	0	0	1	0	0	0	1	Apply	4
A \ BC	00	01	11	10														
0	1	0	0	0														
1	0	0	0	1														
13	Solve the following using NAND gates? a) $(A+B)(C+D)$ b) $A.B+CD(AB^1+CD)$	Apply	4															
14	Sketch the following equation using k-map and realize it using NAND gate? $Y = \sum m(4,5,8,9,11,12,13,15)$	Apply	5															
15	Solve $Y = AB^1 + CD + (A^1B + C^1D^1)$ using NAND gate?	Apply	4															
16	State that AND-OR network is equivalent to NAND-NAND network?	Knowledge	4															
17	Show both NAND and NOR gates are called Universal gates?	Apply	4															
18	Sketch the following logic function using k-map and implement it using logic gates? $Y(A,B,C,D) = \sum m(0,1,2,3,4,7,8,9,10,11,12,14)$	Apply	5															
19	Summarize the rules and limitations of K-map simplification?	Understand	5															
20	Analyze the steps for simplification of POS expression?	Apply	4															
UNIT-III																		
COMBINATIONAL CIRCUITS																		
1	Explain the design procedure for combinational circuits?	Understand	7															
2	Apply various code conversion methods?	Apply	7															
3	Design a 4-bit binary to BCD converter?	Understand	7															
4	Design and implement a 8421 Gray code converter?	Understand	7															
5	Design a combinational logic circuit with 3 input variables that will produce logic 1 output when more than one input variables are logic 1?	Understand	7															
6	Compose and explain the block diagram of 4-bit parallel adder?	Understand	7															
7	Design a logic circuit to convert BCD and gray code?	Understand	7															

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
8	Design a full adder using two half adders?	Understand	7
9	Explain magnitude comparator? Design a 3-bit comparator using logic gates?	Understand	7
10	Compose the circuit for 3 to 8 decoder and explain it with logic gate?	Understand	7
11	Construct the logic circuit for full subtractor using decoder?	Understand	7
12	Define binary decoder? Explain the working of 2:4 binary decoder?	Knowledge	7
13	Design Full adder using a suitable Decoder?	Apply	7
14	Define encoder? Design octal to binary encoder?	Knowledge	7
15	Design a 4-bit priority encoder?	Understand	7
16	Design the block diagram of a 4:1 multiplexer using 2:1 multiplexer?	Understand	7
17	Summarize the following Boolean function using 8:1 mux $F(A,B,C,D)=\pi M(0,3,5,8,9,10,12,14)$	Knowledge	7
18	Explain how decoder acts as a demultiplexer?	Understand	7
19	Differentiate multiplexer and demultiplexer?	Apply	7
20	Explain the working of 8:1 multiplexer?	Understand	7
UNIT-IV			
SYNCHRONOUS SEQUENTIAL CIRCUITS			
1	Differentiate combinational and sequential logic circuits?	Apply	6
2	Explain basic difference between a shift register and counter?	Understand	6
3	Illustrate applications of shift registers?	Apply	6
4	Define bidirectional shift register?	Knowledge	6
5	Describe dynamic shift register?	Knowledge	6
6	Define What is a UART?	Knowledge	6
7	Classify the basic types of counters?	Understand	6
8	Differentiate the advantages and disadvantages of ripple counters?	Apply	6
9	Explain what do you mean by terminal count?	Understand	6
10	Explain what is a variable modulus counter?	Understand	6
11	Design and explain gated latch logic diagram?	Understand	8
12	Define race around condition? How it can be avoided?	Knowledge	8
13	Convert a JK Flip Flop to i) SR ii) T iii) D	Understand	6
14	Convert a SR Flip-Flop to i) JK ii) D iii) T	Understand	6
15	Explain what is a synchronous latch?	Understand	6
16	Construct a latch using universal gates?	Apply	8
17	Explain what do you mean a stable state?	Understand	8
18	Define a Flip-Flop?	Knowledge	6
19	Define applications of Flip-Flops?	Knowledge	6
20	Explain what is meant by clocked flip-flop?	Understand	6
UNIT-V			
MEMORY			
1	Explain the block diagram of memory unit?	Understand	9
2	Explain in detail about RAM and types of RAM?	Understand	9
3	Illustrate the features of a ROM cell?	Apply	9
4	Explain in detail about ROM and types of ROM?	Understand	9
5	Explain coincident memory decoding?	Understand	9
6	Describe what is meant by memory expansion? Mention its limits?	Understand	9
7	List a note on magnetic tape?	Knowledge	9
8	State the advantages and disadvantages of magnetic tape and magnetic disk?	Knowledge	9
9	Differentiate static and dynamic RAM?	Apply	9
10	Explain what is the use of cache memory?	Understand	9
11	Design and explain the following mapping techniques of cache: a) Direct mapping b) Associative mapping	Understand	9

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
12	Explain different replacement algorithms in detail?	Understand	9
13	Explain LRU algorithm in detail?	Understand	9
14	List and explain write policies used with cache memory?	Knowledge	9
15	List a note on performance issues of multilevel memory?	Knowledge	9
16	Explain HIT and MISS ratio in cache memory?	Understand	9
17	Explain the use of an associative-mapped TLB?	Understand	9
18	Design and explain how cache read operation is executed?	Understand	9
19	Explain PLA with the help of block diagram?	Understand	9
20	Explain the advantage of PLA over ROMs?	Understand	9

Group - II (Long Answer Questions)

S. No	Question	Blooms Taxonomy Level	Course Outcome
UNIT-I			
DIGITAL SYSTEMS			
1	(a) Solve the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: i. $100 - 110000$ ii. $11010 - 1101$. (b) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code .Write short notes on binary number systems.	Apply	1
2	(a) Solve arithmetic operation indicated below. Follow signed bit notation: i. $001110 + 110010$ ii. $101011 - 100110$. (b) Explain the importance of gray code?	Apply	1
3	Solve $(3250 - 72532)_{10}$ using 10's complement?	Apply	1
4	As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. Green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. Red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Design a circuit to meet this requirement?	Understand	1
5.	Solve (a) Divide 01100100 by 00011001 (b) Given that $(292)_{10} = (1204)_b$ determine `b'	Apply	1
6.	Solve (a) What is the gray code equivalent of the Hex Number 3A7 (b) Find the biquinary number code for the decimal numbers from 0 to 9 (c) Find 9's complement $(25.639)_{10}$	Apply	1
7.	Solve (a) Find $(72532 - 03250)$ using 9's complement. (b) Show the weights of three different 4 bit self complementing codes whose only negative weight is - 4 and write down number system from 0 to 9.	Apply	1
8.	Decimal system became popular because we have 10 fingers. A rich person On earth has decided to distribute Rs. one lakh equally to the following persons from various planets. Find out the amount each one of them will get in their respective currencies: A from planet VENUS possessing 8 fingers B from planet MARS possessing 6 fingers C from planet JUPITER possessing 14 fingers D from planet MOON possessing 16 fingers	Apply	1
9.	State and prove any 4 Boolean theorems with examples?	Knowledge	3

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10.	Solve a) Simplify to a sum of 3 terms: $A'C'D'+AC'+BCD+A'CD'+A'+AB'C'$ Given $AB' + AB = C$, Show that $AC' + A'C = B$	Apply	4
11	Convert 10101101.0111 to octal equivalent and hexadecimal equivalent?	Understand	1
12	Apply the representation of +65 and -65 in sign magnitude, Sign 1's complement and sign 2's complement representation?	Apply	1
13	State different ways for representing the signed binary numbers?	Knowledge	2
14	Solve addition and subtraction of (456) ₈ and (341) ₈ ?	Apply	1
15	Define weighted codes and non weighted codes with examples?	Knowledge	1
16	Explain what do you mean by error detecting and correcting codes?	Understand	3
17	Illustrate the rules for XS3 addition and subtraction?	Apply	2
18	Explain error occurred in the data transmission can be detected using parity bit?	Understand	3
19	Illustrate IEEE standard floating formats for 32-bit and 64 bit with following examples?	Apply	1
20	Explain the truth tables of X-OR, NAND and NOR gates?	Understand	2
UNIT-II			
GATE LEVEL MINIMIZATION AND COMBINATION CIRCUITS			
1.	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input i. state the minterm expansion for the X,Y,Z ii. state the maxterm expansion for the Y and Z	Knowledge	3
2.	A combinational circuit has four inputs (A,B,C,D), which represent a binary-coded-decimal digit. The circuit has two groups of four outputs - S,T,U,V(MSB digit) and W,X,Y,Z.(LSB digit)Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. Illustrate the minimum expression for all the outputs?	Apply	3
3.	Summarize the following Boolean expressions using K-map and implement them using NOR gates: (a) $F(A, B, C, D) = AB'C' + AC + A'CD'$ (b) $F(W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.$	Understand	4
4.	Design BCD to Gray code converter and realize using logic gates?	Understand	4
5.	Design 2*4 decoder using NAND gates?	Understand	4
6.	compile the following expression using Karnaugh map ($B'A + A'B + AB'$)	Understand	5
7.	Design a circuit with three inputs(A,B,C) and two outputs(X,Y) where the outputs are the binary count of the number of "ON" (HIGH) inputs?	Understand	4
8.	Implement the INVERTER gate, OR gate and AND gate using NAND gate, NOR gate?	Understand	3
9.	Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7?	Understand	4
10.	Implement Half adder using 4 NAND gates?	Understand	3
11	Implement the Boolean function $F = AB + CD + E$ using NAND gates only?	Understand	3
12	Summarize the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15) + d(w, x, y, z) = \Sigma(0, 2, 5)$	Understand	4
13	Construct the logic diagram of a full subtractor using only 2-input NAND gates?	Apply	3
14	Construct the logic diagram of a full subtractor using only 2-input NOR gates?	Apply	3
15	Use a multiplexer having three data select inputs to solve the logic for the function $F = \Sigma(0, 1, 2, 3, 4, 10, 11, 14, 15)$	Apply	4
16	Identify all the prime implicants and essential prime implicants of the	Knowledge	5

S. No	Question	Blooms Taxonomy Level	Course Outcome
	following functions Using karnaugh map. $F(A,B,C,D) = \Sigma(0,1,2,5,6,7,8,9,10,13,14,15)$.		
17	Construct a 4 to 16 line decoder using 2 to 4 line decoders?	Apply	3
18	Design a 4-bit Combinational circuit which generates the output as 2's complement of input binary number. Show that the circuit can be constructed with EX-OR gates?	Understand	3
19	Design a combinatorial circuit that converts a decimal digit from 2,4,2,1 code to the 8,4,-2,-1 code?	Understand	4
20	Design a combinatorial circuit that accepts a three bit number and generates an output Binary number equal to the square of the input number?	Understand	4
UNIT-III			
COMBINATIONAL CIRCUITS			
1.	Design a combinational circuit that generates the 9's complement of BCD digit?	Understand	7
2.	Design a combinational circuit to find the 2's complement of given binary number and realize using NAND gates?	Understand	7
3.	Design a logic circuit to convert gray code to binary code?	Understand	7
4.	Design circuit to detect invalid BCD number and implement using NAND gate only?	Understand	7
5.	Explain the design procedure for code converter with the help of example?	Understand	7
6.	Construct half subtractor using NAND gates?	Apply	7
7.	Design an 8-bit adder using two 74283?	Understand	7
8.	Explain the working of carry look-ahead generator?	Understand	10
9.	Explain carry propagation in parallel adder with neat diagram?	Understand	7
10.	Explain the circuit diagram of full subtractor and full adder?	Understand	7
11.	Construct and explain the working of decimal adder?	Apply	7
12.	Design 2-digit BCD adder with the help of binary adders?	Understand	7
13.	Design Multiply 011_2 by 110_2 using binary multiplication method?	Understand	7
14.	Design 4-bit comparator using logic gates?	Understand	7
15.	State the procedure to implement Boolean function using decoder and also mention the uses of decoders?	Knowledge	7
16.	Design and implement a full adder circuit using a 3:8 decoder?	Understand	7
17.	Describe the operation performed by the following logic circuit with an example. Encoder?		7
18.	Design and Implement full adder circuit using Quadruple 2 to 1 multiplexer?	Understand	7
19.	Construct 16:1 multiplexer using 8:1 and 2:1 multiplexer?	Apply	7
20.	Construct a full adder using a suitable multiplexer?	Apply	7
UNIT-IV			
SYNCHRONOUS SEQUENTIAL CIRCUITS			
1.	Explain the design of Sequential circuit with an example. Show the state reduction, state assignment?	Understand	6
2.	Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers?	Understand	6
3.	Explain about Binary Ripple Counter? What is MOD counter?	Understand	10
4.	Define BCD Counter and Draw its State table for BCD Counter?	Knowledge	6
5.	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in the above process?	Understand	10
6.	Design a sequential circuit with two D flip-ops A and B. and one input x. when $x=0$, the state of the circuit remains the same. When $x=1$, the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00. and repeats?	Understand	6
7.	Design a Modulo-12 up Synchronous counter Using T-Flip Flops and draw	Understand	6

S. No	Question	Blooms Taxonomy Level	Course Outcome
	the Circuit diagram?		
8.	Explain the Ripple counter design. Also the decade counter design?	Understand	10
9.	Design a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter?	Understand	6
10	Design a left shift and right shift for the following data 10110101?	Understand	6
11	Design Johnson counter and state its advantages and disadvantages?	Understand	6
12	Explain with the help of a block diagram, the basic components of a Sequential Circuit?	Understand	6
13	Explain about RS and JK flip-flops?	Understand	6
14	Define T – Flip-flop with the help of a logic diagram and characteristic table?	Knowledge	6
15	Define Latch. Explain about Different types of Latches in detail?	Knowledge	6
16	Illustrate pulse mode asynchronous circuit?	Apply	10
17	List the characteristic equations for all Flip-Flops?	Knowledge	6
18	Construct the transition table for the following flip-flops i) SR FF ii) D FF	Apply	6
19	Describe the steps involved in design of asynchronous sequential circuit in detail with an example?	Understand	10
20	Differentiate critical and non critical race conditions?	Apply	10
UNIT-V			
MEMORY			
1.	List How many address bits are needed to operate a 2 K *8 ROM?	Knowledge	9
2.	Construct a logic diagram of memory cell?	Apply	9
3.	Distinguish between SRAM and DRAM and draw static RAM cell?	Understand	9
4.	Explain the read and write operation a RAM can perform?	Understand	9
5.	Explain the DRAM organization of 2M*8 memory chip?	Understand	9
6.	Construct the signals of a 32*8 RAM with control input. Show the external connections necessary to have a 128*8 RAM using decoder and replication of this RAM?	Apply	9
7.	A block set associative cache consists of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consists of 128 words of 16 bits length? list many bits are there in main memory list many bits are there in each of TAG,SET, and WORD fields?	Knowledge	9
8.	Explain the following terms: i) Cache updation policies. ii)cache hit and cache miss.	Understand	9
9.	Explain two way set associative mapping and four way set associative mapping techniques with an example for each?	Understand	9
10.	Explain how a program gets executed faster using a cache memory?	Understand	9
11	Design a BCD to Excess-3 code converter and implement using Suitable PLA?	Understand	9
12	Construct the block diagram of PLA. Which are the teams programmable? How inverter is useful in PLA construction at the output?	Apply	9
13	Sketch the PLA program table for the four Boolean functions. Minimize the number of product terms? $A(x,y,z)=\sum(0,1,3,5)$ $B(x,y,z)=\sum(2,6)$ $C(x,y,z)=\sum(1,2,3,5,7)$ $D(x,y,z)=\sum(0,1,6)$	Apply	9
14	Sketch a PLA circuit to implement the logic functions $A^1BC+AB^1C+AC^1$ and $A^1B^1C^1+BC$.	Apply	9
15	Explain in detail various cache memory organizations?	Understand	9
16	In many computers the cache block size is in the range 32 to 128 bytes.	Understand	9

S. No	Question	Blooms Taxonomy Level	Course Outcome
	Explain What would be the main advantages and disadvantages of making the size of cache blocks larger or smaller?		
17	Explain the techniques used to perform the write operations in cache memory?	Understand	9
18	Explain about the cache replacement algorithms?	Understand	9
19	Differentiate PAL with PLA with following examples?	Understand	9
20	“Memory hierarchy design is based on the principle of Locality of reference”. Explain the principle?	Understand	9

Group - III (Analytical Questions)

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
UNIT-I			
DIGITAL SYSTEMS			
1.	In a 32 bit computer, what are the maximum and minimum possible binary numbers? Convert these into maximum and minimum possible positive decimal numbers?	Understand	1
2.	Convert the octal numbers into binary, decimal, BCD and Hexadecimal numbers (3600)octal, (1200)octal, (0200)octal, (0777)octal.	Understand	1
3.	Convert the decimal numbers into binary, BCD and Hexadecimal numbers (3600)d, (1200)d, (0200)d, (0777)d.	Understand	1
4.	Suppose you have a cheque for RS.10000/-. what is the number system used? Define base system used and what are the weights of the digits 1,0,0,0,0 and 0 now?	Knowledge	1
5.	Illustrate why is (0.5252)octal twice of (0.2525)octal when (0.5050)d is twice of (0.2525)d.	Apply	1
6.	write the octal representation of the following fractional numbers: (0.5)d, (1.5)d, (2.333)d, (3.875)d, (13.125)d, (14.666)d.	Understand	1
7.	Find the illegal representation in the following: (120A)d, (1010011)BCD, (0208)octal, (10102011)b, (GC0A)h.	Understand	1
8.	Convert the binary number to hexadecimal number: 0100001011010011, 010110101001111.	Understand	1
9.	Convert the hexadecimal number to binary number: 0x5A9F, 42D3.	Understand	1
10	Understand by two examples that two's complement of a number taken twice returns the original number?	Understand	2
UNIT-II			
GATE LEVEL MINIMIZATION AND COMBINATION CIRCUITS			
1.	Use De-morgan theorem to simplify $F = A + B + C.D.E$.	Apply	3
2.	State that for constructing XOR from NANDs we need four NAND gates?	Knowledge	3
3.	State $X + (Y.Z) = (X+Y).(X+Z)$ a distributive law using De-Morgan theorem?	Knowledge	5
4.	Convert $A.B.C + A.D$ expression into standard SOP format?	Understand	4
5.	Convert $(A+B+C).(A+D)$ expression into standard POS format?	Understand	4
6.	Construct XOR from NOR gates?	Understand	3
7.	Construct SOP expression and POS expression for a four input NAND gate?	Understand	4
8.	Understand Excess-3 codes for 3 and 7?	Understand	3
9.	Find the logic function F using AND-OR two level realization?	Understand	4
10	Find transmitted 11 bits for 0110001 when hamming code is used?	Understand	4

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UNIT-III			
COMBINATIONAL CIRCUITS			
1.	Design a combinational logic circuit that produces the product of 2 binary number ? $A=(A_1, A_0) * B=(B_2, B_1, B_0)$	Understand	7
2.	Solve the function using multiplexer $F(x,y,z)=\sum(0,2,6,7)$	Apply	7
3.	A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input: i. Find the minterm expansion for the X,Y,Z ii. Find the maxterm expansion for the Y and Z	Understand	7
4.	Design a combinational logic circuit with 4 inputs A, B, C, D. The output Y goes High if and only if A and C inputs go High. Draw the truth table. Minimize the Boolean function using K-map. Draw the circuit diagram?	Understand	7
5.	Design a logic circuit to convert excess-3 code to BCD code?	Understand	7
6.	Design a 24-bit group ripple adder using 74X283 ICs?	Understand	7
7.	Design a multiple circuit to multiply the following binary number $A=A_0A_1A_2$ and $B=B_0B_1B_2B_3$ using required number of binary parallel adders?	Understand	7
8.	Solve the following Boolean functions using decoder and OR gates: $F_1(A,B,C,D)=\sum(2,4,7,9)$ $F_2(A,B,C,D)=\sum(10,13,14,15)$	Apply	7
9.	Design the interfacing diagram of 10 key keypad interfaces to digital system using decimal to BCD encoder?	Understand	7
10.	Solve the following Boolean function using 4:1 mux $F(A,B,C,D)=\sum m(1,3,5,7,8,9,0,2,10,12,13)$	Apply	7
UNIT-IV			
SYNCHRONOUS SEQUENTIAL CIRCUITS			
1.	Explain the output frequency of T flip-flop if the input clock frequency is 10khz? Give its timing waveform?	Apply	6
2.	A sequential circuit has 3 flip-flops, A,B and C and one input ,X .it is described by the following flip flop input functions? $D_A=(BC^1+B^1C)x+(BC+B^1C^1)x^1$ $D_B=A$ $D_C=B$ i) Derive the state table for circuit ii) Draw two state diagrams: One for x=0 and for x=1		6
3.	Design and implement 4-bit binary counter(using D flip flops) which counts all possible odd numbers only?	Understand	6
4.	Find the state assignments for sequence 1101011?	Understand	10
5.	Design 2's complemeter with a shift register and flip flop. The binary number is shifted outside and its 2's complement shifted other side of the shift register?	Understand	6
6.	Design a MOD-5 synchronous counter using flip flops and implement it? Also draw the timing diagram?	Understand	6
7.	Design a divide-by-128 counter using 7493 IC's?	Understand	10
8.	Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0 , The output does not change for any change in X?	Understand	10
9.	Design an asynchronous D-type latch with two inputs G and D output Q. Assume fundamental mode of operation?	Understand	6
10.	Design a T flip flop from logic gates?	Understand	6
UNIT-V			
MEMORY			

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
1.	Solve the following two Boolean functions using a PLA having 3-inputs,4 product terms and 2 outputs? $F_1(A,B,C)=\sum(0,1,2,4)$ $F_2(A,B,C)=\sum(0,5,6,7)$	Apply	9
2.	Design 1k*8 RAM using two 1k*4 IC?	Understand	9
3.	Solve 2048*8 memories using 256*8 memory chip .Also show the memory address associated with each memory chip?	Apply	9
4.	Calculate the utilization factor of tape, if the gap length is 0.5 in, the storage density $S=3000$ bytes/in and data storage capacity is 6 k bytes?	Apply	9
5.	A two way set associative cache memory uses block of four words. The cache accommodate a total of 2048 words from main memory. The main memory size is 128k*32 i) Find how many bits are there in tag index, block and word field of address format? ii) Find the size of cache memory?	Understand	9
6.	Solve the following multi boolean function using 3*4*2 PLA PLD? $F_1(a_2, a_1, a_0)=\sum m(0,1,3,5)$ $F_2(a_2, a_1, a_0)=\sum m(3,5,7)$	Apply	9
7.	Design and implement 3-bit binary to gray code converter using PLA?	Understand	9
8.	Calculate the average access time of memory for a computer with cache access time of 100ns,a main memory access of 1000ns and a hit ratio is 0.9?	Apply	9
9.	A direct mapped cache has the following parameters: cache size=1k words, Block size=128 words and main memory size is 64 k words. Find the number of bits in TAG, WORD and BLOCK in main memory address?	Understand	9
10	Design a combinational circuit using PLA. The circuit accepts 3-bit number and generates an output binary number equal to square of input number?	Understand	9