1. Group - A (Short Answer Questions)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
	UNIT-I **OPERATIONAL AMPLIFIER**		
1	Mention the advantages of integrated circuits.	Remember	1,2
2	write down the various processes used to fabricate IC's using silicon planar technology.	Analyze	1,2
3	What is the purpose of oxidation?	Analyze	1,2
4	Why aluminum is preferred for metallization?	Remember	1,2
5	Define an operational amplifier.	Analyze	1
6	Mention the characteristics of an ideal op-amp.	Analyze	1
7	Define input offset voltage	Remember	1
8	What are the applications of current sources?	Remember	1
9	Define sensitivity. Mention the advantages of Wilson current source	Remember	1,2

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
10	What is a current mirror? Explain the working of a wilder current source		
11	What is slew rate? Discuss the methods of improving slew rate.	Remember	1
12	What is an Active load? Explain the CE amplifier with active load	Remember	1
13	Explain pole zero compensation and frequency compensation in op-amp.	Analyze	1,2
14	Define band gap reference? Explain in detail about the reference circuit		
15	Briefly explain the method of using constant current bias for increasing CMRR in differential?	Understand	1,2
16	Explain the operation of a Schmitt trigger circuit		
17	Explain the working of full precision rectifier?		
18	Define ripple rejection with respect to voltage regulators	Analyze	1
	UNIT-II **OP-AMP, IC -555 & IC 565 APPLICATIONS**		
1	Why active filters are preferred?	Remember	2
2	What is meant by cut off frequency of a high pass filter and how it is found out in a first order high pass filter	Understand	2
3	List the applications of 555 timer in monostable mode of operation	Remember	2
4	Define 555 IC?	Remember	2
5	List the basic blocks of IC 555 timer?	Remember	2
6	Define VCO.	Remember	2
7	What does u mean by PLL?	Understand	2
8	List the applications of 565 PLL	Apply	2
9	Define lock range.	Understand	2
10	Define capture range	Apply	2
11	Define pull-in time	Understand	2
	UNIT-III **DATA CONVERTERS**		
1.	List the broad classification of ADCs	Remember	3
2.	List out the direct type ADCs	Understand	3
3.	List out some integrating type converters	Remember	3
4.	What is integrating type converter	Understand	3
5.	Explain in brief the principle of operation of successive Approximation ADC	Analyze	3
6.	What are the main advantages of integrating type ADCs	Understand	3
7.	What is the main drawback of a dual-slop ADC?	Remember	3
8	Define conversion time.	Remember	3
9.	Define accuracy of converter	Remember	3
10.	Explain in brief stability of a converter	Remember	3
	UNIT-IV **DIGITAL INTERAGETED CIRCUITS**		

S. No	QUESTION	Blooms Taxonomy Level	Course Outcome
1.	Explain how PROM, EPROM and EEPROM technologies differ from each other.	Analyze	10
2.	Design CMOS transistor circuit for 2-input AND gate.	Understand	4
3.	Explain sourcing current of TTL output?	Remember	4
4.	Which of the parameters decide the fan-out and how?	Understand	4
5.	Explain sinking current of TTL output?	Understand	4
6.	Explain the term Voltage levels for logic '1' & logic '0' with reference to TTL gate?	Understand	4
7.	Explain the DC Noise margin with reference to TTL gate?	Understand	4
8.	Explain Low-state unit load with reference to TTL gate?	Remember	4
9.	Explain High-state fan-out with reference to TTL gate?	Remember	4
10.	Explain the use of Package?	Remember	4
	UNIT-V **SEQUNTIAL LOGIC ICS AND MEMORIES**		
1.	Define static RAM	Understand	5
2.	Define dynamic RAM	Understand	5
3.	Classify types of ROMs	Understand	5
4.	Applications of ROMS	Remember	5
5.	What is the difference between latch& Flip-Flop, Explain with logic diagram.	Remember	5
6.	Explain any one application of SR latch.	Understand	5
7.	What is race around condition? how it is avoided?	Remember	5
8.	How synchronous counters differ from asynchronous counters?	Understand	5
9.	List counter applications.	Understand	5
10.	State various applications of counters.	Remember	5

2. Group - II (Long Answer Questions)

S. No	Question	Blooms Taxonomy Level	Course Outcome
	UNIT-I **OPERATIONAL AMPLIFIER**		
1.	With circuit diagram discuss the following applications of op-amp(Dec-03) (i) Voltage to current converter(ii)Precision rectifier	Evaluate	1,2
2.	Explain the operation of a Schmitt trigger circuit	Evaluate	1,2
3.	Explain the working of full precision rectifier	Evaluate	1,2
4.	Explain the internal structure of voltage regulator IC 723. Also draw a low voltage Regulator circuit using IC 723andexplain its operation.	Analyze	1,2
5.	Explain the following terms in an OP-AMP. Bias current	Evaluate	1,2

S. No	Question	Blooms Taxonomy Level	Course Outcome
	(1) Thermal drift (2) Input offset voltage and current (3) Thermal drift		
6.	Explain the frequency compensation techniques of OP-AMP	Evaluate	1,2
7.	Draw the circuit of a symmetrical emitter coupled differential amplifier and derive for CMRR.	Evaluate	1,2
8.	Write a technical note on frequency response characteristics of differential amplifier. State the importance of frequency compensation	Analyze	1,2
9.	What is t instrumentation amplifier? What are the required parameters of an instrumentation amplifier? Explain the working of instrumentation amplifier with neat circuit diagram	Understand	1,2
10	Explain various DC and AC characteristics of an op.amp. Distinguish between ideal and practical characteristics	Remember	1,2
11	With circuit and waveforms explain the application of OPAMP as (1) Integrator (2) Voltage series Feedback Compensation	Evaluate	1,2
	UNIT-II **OP-AMP, IC -555 & IC 565 APPLICATIONS**		
1.	Design a second order low pass filter	Evaluate	4
2.	Draw the circuit of a 1st order Butterworth low pass filter and derive its transfer function.	Analyze	4
3.	Explain the functional block diagram of 555timer	Evaluate	4
4.	Explain working of PLL using suppropriate block diagram and explain any one application of the same	Evaluate	4
5.	Draw the block diagram of an Astable multivibrator using 555timer and derive an expression for its frequency of oscillation	Evaluate	4,5
6.	Draw the block diagram of monostable multivibrator using 555timer and derive an expression for its frequency of oscillation	Evaluate	4,5
7.	write short notes on i) capture range ii) Lock in range iii) Pull in time	Analyze	4,5
8.	Explain about power amplifier and video amplifier	Analyze	4,5
9.	Draw the circuit of a 1st order Butterworth high pass filter and derive its transfer function	Analyze	4,5
10.	Explain Band pass ,band reject and all pass filters	Analyze	4,5
	UNIT-III **DATA CONVERTERS**		
1.	Explain the working of a Weighted resistor D/A converter	Evaluate	8
2.	Explain successive approximation A/D converter	Understand	8
3.	Explain the working of a dual slope A/D converter	Remember	8
4.	Explain the working of a Voltage to Time converter	Understand	8
5.	Explain the working of a counter type A/D converter and state it's important feature	Understand	8
6.	Explain the working of a Voltage to Frequency converter	Understand	8

S. No	Question	Blooms Taxonomy Level	Course Outcome
7.	Explain the working of a Voltage to Frequency converter	Analyze	8
8.	With neat diagram, explain the working principle of R-2R ladder type DAC	Analyze	7,8
9.	Explain the following application of operational amplifier. (1) peak detector (2) Functions of flash type A/D converter.	Understand	7,8
10.	With neat diagram,explain the workingprinciple of Weighted resistor DAC	Understand	7,8
	UNIT-IV **DIGITAL INTERAGETED CIRCUITS**		
1.	(a) Explain the following terms with reference to CMOS logic. i. Logic Levels ii. Noise margin iii. Power supply rails iv. Propagation delay (b) What is the difference between transmission time and propagation delay? Ex- plain these two parameters with reference to CMOS logic.	Apply	10
2.	(a) Draw the circuit diagram of two-input 10K ECL OR gate and explain its operation. (b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00.	Analyze	10
3.	(a) Discuss the steps in VHDL design flow. (b) Explain the difference in program structure of VHDL and any other procedural language. Give an example	Understand	10
4.	(a) Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table? (b) Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs.	Remember	10
5.	(a) Design a three input NAND gate using diode logic and a transistor inverter?Analyze the circuit with the help of transfer characteristics. (b) Explain sinking current and sourcing current of TTL output? Which of the parameters decide the fan-out and how?	Evaluate	10
6.	(a) Realize the logic function performed by 74×381 with ROM. (b) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow out-put. Show the block schematic with all inputs and outputs.	Evaluate	10
7.	Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.	Evaluate	10
8.	Explain the necessity of two-dimensional decoding mechanism in memories.	Apply	10
9.	With the help of timing waveforms, explain read and write operations of SRAM.	Remember	10
10.	Draw MOS transistor memory cell in ROM and explain the operation.	Apply	10
	UNIT-V **SEQUNTIAL LOGIC ICS AND MEMORIES**		
1.	How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow out-put. Show the block schematic with all inputs and outputs.	Understand	9
2.	Draw the basic cell structure of Dynamic RAM. What is the necessity of	Analyze	9

S. No	Question	Blooms Taxonomy Level	Course Outcome
	refresh cycle? Explain the timing requirements of refresh operation.		
3.	Discuss in detail ROM access mechanism with the help of timing waveforms.	Analyze	9
4.	Draw the logic diagram of 74×163 binary counter and explain its operation.	Understand	10
5.	Design a modulo-100 counter using two 74×163 binary counters?	Apply	10
6.	Design a Modulo-12 ripple counter using 74×74?	Apply	10
7.	Discuss how PROM,EPROM, EEPROM technologies differ from each other?	Analyze	10
8.	Differentiate between ripple counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.	Remember	10
9.	Design a modulo-88 counter using 74X163 Ics.	Understand	

3. Group - III (Analytical Questions)

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
	UNIT-I **OPERATIONAL AMPLIFIER**		
1.	An op-amp with a slew rate = 0.5V/μS is used as an inverting amplifier to obtain a gain of 100. The voltage gain Vs frequency characteristic of the amplifier is flat up to 10 KHz. Determine i. The maximum peak-to-peak input signal that can be applied without any distortion to the output ii. The maximum frequency of the input signal to obtain a sine wave output of 2V peak	Evaluate	1,2
2.	Design a Schmitt trigger for UTP =0.5v and LTP=-0.5V	Analyze	1,2
3.	Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms	Remember	1,2
4.	Determine the output voltage of the differential amplifier having input voltages V1=1mV and V2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000	Remember	1,2
5.	Draw the output waveform for a sine wave of1vpeak at 100Hzapplied to the differentiator	Remember	1,2
6.	Design an op-amp differentiator that will differentiate an Input signal with fmax = 100Hz	Explain	1,2
7.	Determine the input impedance of 741 operational amplifier employed as voltage follower having Av=50,000 and Ri= 0.3MEGA OHM	Remember	1,2
	UNIT-II **OP-AMP, IC -555 & IC 565 APPLICATIONS**		
1.	Design an Astable Multivibrator using 555 Timer to produce 1Khz square wave form for duty cycle=0.50	Evaluate	3,4
2.	Design and draw the wave forms of 1KHZ square waveform generator	Evaluate	3,4

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
	using555 Timer for duty cycle i)D=25% ii) D=50%		
3.	Design a 555 based square wave generator to produce an asymmetrical square wave of 2 KHz. If Vcc=12V, draw the voltage curve across the timing capacitor and output waveform.	Analyze	3,4
4.	Draw the schematic diagram of an all pass filter and determine the phase shift φ between the input and output at f = 2kHz	Analyze	3,4
	UNIT-III **DATA CONVERTERS**		
1.	A dual slope ADC uses a16-bitcounteranda 4MHzclock rate. The maximum input voltage is+10v. The maximum integrator output voltage should be-8v when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1 µF Find the value of the resistor R of the integrator.	Apply	7,8
2.	Find the voltage at all nodes 0,1,2,…. And at the output of a 5-bit R-2R ladder DAC. The least Significant bit is 1 and all other bits are equal to 0. Assume VR = -10V and R=10KO.	Remember	7,8
3.	A dual slope ADC uses an 18 bit counter with a 5MHz clock. The maximum integrator input voltage in +12V and maximum integrator output voltage at 2n count is -10V. If R=100KO, find the size of the capacitor to be used for integrator	Understand	7,8
4.	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111	Apply	7,8
5.	Calculate the values of the LSB,MSB and full scale output for an 8 bit DAC for the 0 to 10V range	Apply	7,8
6.	An ADC converter has a binary input of 0010 and an analog output of 20mv. What is the resolution	Apply	7,8
7.	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 3V	Apply	7,8
8.	Calculate what is the conversion time of a 10 bit successive approximation A/D converter if its 6.85V	Remember	7
9.	A dual slope uses a 16 bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1µf. Find the value of the resistor R of the integrator	Apply	7
10	Analyze the fall time of CMOS inverter output with RL = 100, VL = 2.5V and CL=10PF. Assume VL as stable state voltage.	Apply	7
11	Design the logic circuit and write a data-flow style VHDL program for the following function .F (R) = A,B,C,D (1, 4, 5, 7, 9, 13, 15)	Analyze	7,8
12	A simple floating-point encoder converts 16-bit fixed-point data using four high order bits beginning with MSB. Design the logic circuit and write VHDL data-flow program.	Remember	7,8
13	Design a 4-bit binary synchronous counter using 74×74. Write VHDL program for this logic. Using data flow style	Analyze	7,8
14	Draw the logic diagram of 74×163 binary counter and explain its operation.	Remember	7,8
15	Design a modulo-100 counter using two 74×163 binary counters?	Understand	7,8
16	A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor?	Analyze	7,8

S.No	QUESTIONS	Blooms Taxonomy Level	Course Outcome
	How much high state DC noise margin can be provided in this case?		
	UNIT-IV **DIGITAL INTERAGETED CIRCUITS**		
1.	Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.	Apply	9,10
2.	Realize the logic function performed by 74×381 with ROM.	Evaluate	9
3.	Explain the internal structure of 64K×1 DRAM with the help of timing diagrams.	Apply	9
4.	Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.	Apply	9