VLSI Design

Unit-1:

1. a). Explain the fabrication steps of twin -tub process for CMOS technology?
   b). Distinguish between bipolar, CMOS transistor technologies.
2. a). Draw the structure of nMOS transistor and explain how I_{ds}, depends on W/L ratio
   b). What is Latch-up in CMOS circuits? How to overcome it?
3. a). Explain the various fabrication steps for pMOS technology with neat diagrams.?
   b). Discuss the Microelectronics evolutionary process with examples.
4. a). Discuss fabrication differences between NMOS and CMOS technologies. Which fabrication is preferred and why?
   b). Derive the relation between pull-up and pull -down ratio for an nMOS inverter driven through one or more pass transistors.

Unit-2:

1. a). What are the Lambda -based design rules? Give some examples.
   b). Design and Draw the Layout of CMOS NAND gate and explain its working.
2. a). Explain the design rules for wires and contacts.
   b). Design and Draw the Layout of CMOS NOR gate and explain its working.
3. a). Design a stick diagram for two input CMOS NAND and NOR gates.
   b). Explain the Transistor design rules for nMOS. pMOS and CMOS technologies
4. a). What are the different steps in the stick layout using nMOS design?
   b). Explain CMOS lambda based design rules.

Unit-3:

1. a). How do you estimate the rise -time and fall -time of CMOS inverter?
   b). Explain how to drive large capacitive loads?
2. a). How do you estimate the rise -time and fall -time of CMOS inverter?
   b). Explain how to drive large capacitive loads?
3. Explain the following with suitable examples:
   (a) Sheet resistance
   (b) Inverter delays
   (c) Propagation delays
4. a). Explain how MOSFETs can be used as switches.
   b). what is inverter delay? How delay is calculated for multiple stages?

Unit-4:

1. (a)Explain pass transistor logic and Transmission gate logic with one example.
   (b)Draw the circuits of two input NAND Gate using nMOS, CMOS and BiCMOS logic.
2. (a) Draw the circuits of two input NOR Gate using nMOS, CMOS and BiCMOS logic.
   (b).Explain pseudo nMOS NAND gate.
3. (a)Explain Dynamic CMOS NAND gate.
   (b).Explain CMOS Domino Logic.
4. (a).Design 4×1 MUX with nMOS switches.
   (b).Explain two phase clocking technique with any two generation methods.
5. (a)Explain various system considerations in a leaf –cell design.
   (b)Illustrate the subsystem design process with an example.

Unit-5:

1. What is a Dynamic Power and Static Power.
2. Write the advantages and disadvantages of cell based and array based Design.
3. Explain the stuck at fault model with example.
4. Give the two reasons about the importance of package selections.
5. Explain about the clocking mechanism and define the term clock skew.

Unit-6:

1. Explain the basic architecture of FPGA.
2. Explain the functions of LUT based Logic block and Multiplexer based Logic block.
3. Explain the design flow of FPGAs.
4. Write the VHDL code to Implement Stack/Queue.
5. . Write the VHDL code to implement 4-Bit Shift Register.