DSD&DICA

Unit-I:

1. a) What is HDL? Why do you need it?
   b) Give the syntax and structure of a package in VHDL.

2. a) Explain about dataflow design elements of VHDL.
   b) Differentiate between VHDL and Verilog HDL.

3. a) What are different data types available in VHDL? Explain.
   b) Explain about data objects in VHDL

4. a) Discuss the binding? Discuss the binding between entity and components.
   b) Explain about signal assignment statements and Variable assignment statements with example.

5. a) Explain the structure of various LOOP statements in VHDL with examples
   b) Write a VHDL program for n-bit ripple carry adder

Unit-II:

1. a) Define simulation? Explain about Gate-level simulation, Behavioral simulation and Functional simulation.
   b) Explain about inertial delay and Transport delay models in VHDL with examples.

2. a) What are the goals and objectives of Global routing and detailed routing?
   b) Explain the following:
      i) Timing constraints
      ii) Performance-driven synthesis
      iii) Circuit – level simulation.

3. a) What is the importance of time dimension in VHDL and explain its function.
   b) Discuss some of the important factors related to Synthesis.

4. a) Write a VHDL program for comparing 8 bit unsigned integers.
   b) Discuss synthesis information from entity with examples.

5. a) Write a test bench for two input XOR gate using VHDL.
b) Write a VHDL program for 2x4 Decoder

Unit-III:

1. a) What are advantages of Programmable logic devices?

b) Compare PROM, PAL and PLA.

2. a) With the help of timing waveforms, explain the read and write operations of static RAM.

b) Distinguish between SRAM and ROM.

3. a) Draw the block diagram of Synchronous RAM and explain its operation.

b) Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.

4. a) Describe DRAM with an appropriate diagram and explain about its timings.

b) Design an excess-3 to BCD code converter using PLA.

5. a) Implement the following Boolean functions using a PLA

F1(A,B,C)= _ m(0,1,3,5); F2=(A,B,C)= _ m(3,5,7).

b) Design a BCD to Gray-code converter using PLA.

Unit-IV:

1. a) Give the logic levels and noise margins of CMOS and TTL families.
   b) What are the advantages and disadvantages of CMOS technology?

2. a) Explain the CMOS circuit behavior with resistive load.
   b) Design a 2-input XOR and XNOR logic gates using CMOS logic.

3. a) Explain about the steady state electrical CMOS behaviors for
      i) Resistive loads ii) Non ideal inputs
   b) Design a 4 input CMOS OR-AND INVERT gate. Explain the circuit with the help of logic diagram and function table.

4. a) Design a 4 input CMOS AND-OR-INVERT gate. Explain the circuit with the help of logic diagram and function table.
   b) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.

5. a) What is interfacing? Explain interfacing between low voltage TTL and low voltage CMOS logic.
   b) Design a transistor circuit of 2 input ECL NOR gate. Explain the operation with the help of function table

Unit-V:

1. a) Write a VHDL program for 4x2 encoder.

   b) Write a VHDL program for 4x1 multiplexer

2. a) Design a full adder using two half adders. Write VHDL program for the above implementation.

   b) Design a 16-bit comparator using 74×85IC's.

3. a) Implement the 32 input to 5 output priority encoder using four 74LS148 & gates.

   b) Draw the logic diagram of IC 74180 parity generator checker and explain its operation with the help of a truth table.

4. a) Write a VHDL code for 4-bit Look ahead carry generator.

   b) Design a 4×4 combinational multiplier and write the VHDL program in data flow model.

5. a) Design a priority encoder for 16 inputs using two 74×148 encoders.

   b) Write the VHDL program for fixed point to floating point conversion.

Unit-VI:

1. a) Convert a JK Flip-flop into D Flip-flop.

   b) Convert a T flip-flop into a D Flip-flop

2. a) Explain how a JK- flip-flop can be constructed using a T- flip-flop.

   b) Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style.

3. a) Design an Excess-3 decimal counter using 74 X 163 and explain the operation with the help of timing waveforms

   b) Give a VHDL code for a 4-bit upcounter with enable and clear inputs

4. a) Design a 3 bit LFSR counter using 74×194.List out the sequence assuming that the initial state is 111.

   b) Draw the logic diagram of universal shift register and explain its operation.

5. a) Design a 8 bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.

   b) Design a modulo – 100 counter using two 74 x 163 binary counters