GROUP-A (SHORT ANSWER QUESTIONS)

S No.	Questions	Bloom's Taxonomy Level	Course Outcome
	UNIT-I		
1	**Define** oxidation & Classify different types of oxidation	Remember	1
2	**Explain** about Ion implantation	Understand	1
3	**Describe** lithography	Understand	1
4	**List** the advantages of IC	Remember	1
5	**Discuss** the four generations of Integration Circuits	Understand	1
6	**State** the various Silicon wafer Preparations	Remember	1
7	**Describe** BiCMOS Technology	Understand	1
8	**Illustrate** the steps involved in twin-tub process	Remember	1
9	**State** the different types of CMOS process	Remember	1
10	**Describe** encapsulation	Understand	1
11	**Explain** the basic processing steps involved in BiCMOS process	Remember	1
12	**State** Moore's law	Remember	1
13	**Describe** enhancement mode and depletion mode of transistor	Remember	1
14	**State** the advantages of CMOS process	Remember	1

S No.	Questions	Bloom's Taxonomy Level	Course Outcome
15	**Describe** diffusion	Remember	1
16	**List** the advantages of CMOS process	Remember	1
	UNIT – II		
1	**State** why nMOS technology is preferred more than pMOS technology.	Remember	2
2	**Describe** Short Channel devices.	Remember	2
3	**Explain** a pull down device.	Understand	2
4	**Explain** pull up device.	Remember	2
5	**Describe** the different operating regions for an MOS transistor.	Remember	2
6	**Define** Threshold voltage.	Remember	3
7	**State** Body effect.	Remember	3
8	**Describe** Channel length modulation.	Remember	3
9	**Define** Latch up.	Remember	2
10	**Demonstrate** the CMOS inverter circuits.	Apply	3
11	**Demonstrate** nMOS inverter circuit.	Apply	3
12	**Distinguish** between linear and circular convolution of two sequences.	Understand	2
13	**Demonstrate** BiCMOS inverter circuit.	Apply	3
14	**Describe** figure of merit.	Remember	2
15	**Explain** pass transistor.	Understand	2
16	**Demonstrate** the transfer characteristics of CMOS.	Apply	2
	UNIT – III		
1	**Explain** VLSI design flow.	Understand	3
2	**Describe** Stick Diagram.	Remember	3
3	**List** the uses of Stick diagram.	Remember	4
4	**List** the various color coding used in stick diagram.	Remember	4
5	**Explain** different MOS layers.	Understand	4
6	**Sketch** a stick diagram for 2 input nMOS NAND gate.	Apply	4
7	**Sketch** a stick diagram for CMOS inverter.	Apply	4
8	**List** the types of design rules.	Remember	4
9	**Sketch** a Transistor related design rules (Orbit 2 μm CMOS) minimum sizes and overlaps	Apply	5
10	**Sketch** the aspects of λ-based design rules for contacts, including some factors contributing to higher yield/reliability.	Apply	5
11	**Sketch** the stick diagram for 2 i/p nMOS nor gate.	Apply	4
12	**Describe** Scaling.	Remember	5
13	**Explain** about transistor design rules for nMOS.	Understand	5
14	**Describe** layout diagram.	Remember	4
15	**Sketch** stick diagram for nMOS inverter.	Apply	4
	UNIT – IV		
1	**Give** the different symbols for transmission gate	Remember	6
2	**What** is pass transistor?	Understand	6
3	**What** is sheet resistance?	Remember	6
4	**Define** Rise time.	Understand	6

S No.	Questions	Bloom's Taxonomy Level	Course Outcome
5	**Define** Fall time.	Remember	6
6	**Define** Delay time.	Remember	6
7	**What** are the other forms of CMOS logic?	Understand	6
8	**What** is meant by wiring capacitance?	Remember	6
9	**What** is fan in?	Understand	6
10	**What** is fan out?	Understand	6
11	**Draw** OR gate with pass transistors.	Apply	6
12	**Draw** the circuit for inverter type super buffer.	Apply	6
	UNIT – V		
1	**What** is a data path subsystem?	Remember	7
2	**What** is a shifter?	Remember	7
3	**What** is the difference between shifter and barrel shifter?	Remember	7
4	**Write** the truth table for full adder.	Remember	7
5	**Draw** the circuit of one detector with AND gates.	Apply	7
6	**Draw** the circuit of zero detector with AND gates.	Understand	7
7	**What** is comparator?	Remember	7
8	**Draw** the circuit of comparator.	Apply	7
9	**What** is parity generator?	Remember	7
10	**What** is the difference between synchronous and asynchronous counter.	Remember	7
	UNIT – VI		
1	**Write** categories of memory arrays	Understand	8
2	**What** is a RAM	Understand	8
3	**What** is ROM	Understand	8
4	**What** is serial access memory	Understand	8
5	**What** is content Addressable memory	Understand	8
6	**Draw** the 6-Transistor SRAM cell	Apply	8
7	**Draw** the 1-Transistor Dram cell	Apply	8
8	**What** are the different types of serial access memories	Remember	8
9	**What** is flash memory	Remember	8
10	**What** are the different types of ROMs	Remember	8
11	**Explain** the principle of SRAM	Understand	8
12	**Discuss** the advantages of SRAM	Understand	8
13	**Explain** the principle of DRAM	Understand	8
14	**Discuss** the advantages of Flash memory	Understand	8
	UNIT – VII		
1	**Name** the different types of ASICs.	Remember	9
2	**Analyze** full custom ASIC design.	Understand	9
3	**Analyze** the standard cell-based ASIC design.	Understand	9
4	**Differentiate** between channeled & channel less gate array.	Remember	9
5	**Explain** about FPGA.	Understand	9
6	**Explain** about antifuse technology.	Understand	9
7	**Explain** about Programmable Interconnects.	Understand	9

S No.	Questions	Bloom's Taxonomy Level	Course Outcome
8	**List** the steps in ASIC design flow.	Remember	9
9	**Discuss** the parameters influencing low power design.	Understand	9
10	**Explain** about CPLD.	Understand	
	UNIT – VIII		
1	**State** the levels at which testing of a chip can be done.	Remember	10
2	**Discuss** the categories of testing.	Understand	10
3	**Explain** functionality tests.	Understand	10
4	**Explain** manufacturing tests.	Understand	10
5	**Discuss** the defects that occur in a chip	Understand	10
6	**Explain** about fault models	Understand	10
7	**Analyze** stuck – at fault	Understand	10
8	**Explain** fault models with examples	Understand	10
9	**Discuss** about observability	Understand	10
10	**Discuss** about controllability	Understand	10
11	**Explain** various approaches in design for testability	Understand	10
12	**Mention** the common techniques involved in ad hoc testing	Remember	10
13	**Analyze** the scan-based test techniques	Understand	10
14	**Analyze** the self-test techniques.	Understand	10
15	**Discuss** the applications of chip level test techniques.	Understand	10
16	**Explain** boundary scan	Understand	10
17	**Analyze** test access port	Understand	10
18	**Explain** about boundary scan register.	Understand	10

GROUP-B (LONG ANSWER QUESTIONS)

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
	UNIT-I		
1	**Explain** the operation of NMOS enhancement transistor	Understand	1
2	**Explain** about the body effect of MOS transistors.	Understand	1
3	**Explain** the silicon semiconductor fabrication process	Understand	1
4	**Explain** the fabrication of PMOS transistor and its substrate fabrication Process	Understand	1
5	**Explain** different fabrication process of CMOS transistor	Understand	1
6	**Explain** the silicon semiconductor fabrication process	Understand	1
7	**Derive** the threshold voltage for NMOS enhancement transistor	Apply	1
8	**Derive** the design equations for MOS devices	Apply	1
9	**Explain** channel length modulation.	Understand	1
10	**Explain** BiCMOS fabrication in an n-well process	Understand	1
11	**Compare** between CMOS and bipolar technologies	Remember	1
12	**Explain** the oxidation process in the IC fabrication process with sketches.	Understand	1

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
	UNIT – II		
1	**Illustrate** the relationship between I_{ds} versus V_{ds} of MOSFET	Understand	2
2	**Interpret** the Pull-up to pull-down ratio(Z_{pu}-Z_{pd}) for an nMOS inverter driven by another nMOS inverter	Apply	3
3	**Interpret** the Pull-up to pull-down ratio(Z_{pu}-Z_{pd}) for an nMOS inverter driven through One or more Pass Transistors	Apply	3
4	**Explain** the various forms of pull-ups.	Understand	3
5	**Explain** what is latch up in CMOS and BiCMOS Susceptibility.	Understand	3
6	**Differentiate** the parameters of CMOS and Bipolar Technologies	Remember	2
7	**Explain** BiCMOS inverter in all conditions.	Understand	3
8	**Explain** the latch up prevention techniques.	Remember	3
9	**Illustrate** the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics	Apply	3
10	**Explain** the terms figure of merit of MOSFET and output conductance, using necessary equations	Remember	2
	UNIT – III		
1	(a) **What** is a stick diagram? Sketch the stick diagram and layout for a CMOS inverter. (b) **What** are the effects of scaling on Vt. (c) **What** are design rules? Why is metal- metal spacing larger than poly – poly spacing.	Understand	4
2	**Explain** clearly the nMOS Design style with neat sketches.	Understand	4
3	**Explain** clearly the CMOS Design style with neat sketches.	Understand	4
4	**Sketch** the stick diagram for the NMOS implemented of the Boolean expression Y = AB + C.	Apply	4
5	(a) **Sketch** a Schematic and Cell Layout with neat diagrams. (b) With neat diagram explain λ- based design rules for contact cuts and vias.	Apply	5
6	**Sketch** the circuit schematic and stick diagram of CMOS 2-Input NAND gate	Apply	4
7	**sketch** the transistor level diagram for the given expression and also get the corresponding Stick diagram representation in CMOS logic Y = a (b + c) +d	Apply	4
8	**Define** scaling. What are the factors to be considered for transistor scaling?	Remember	2
9	**Define** constant voltage scaling. Give necessary equations.	Remember	5
10	**Explain** with suitable examples how to design the layout of a gate to maximize performance and minimize area.	Remember	4
	UNIT – IV		
1	**Draw** the CMOS implementation of 4-to-1 MUX using transmission gates.	Apply	4
2	**Explain** the VLSI design flow with a neat diagram	Understand	4
3	**Explain** the Transmission gate and the tristate inverter briefly	Understand	4
4	Clearly **explain** the AOI implementation using cmos design style with neat diagrams.	Apply	4
5	**Design** a 2-input multiplexer using CMOS transmission gates.	Apply	4
6	**Explain** PSEUDO nMOS Logic give its advantages and disadvantages	Apply	6
7	**Explain** dynamic CMOS logic give its advantages and disadvantages	Understand	6
8	**Explain** CMOS domino logic give its advantages and disadvantages	Understand	6

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
9	**Explain** clocked CMOS logic and n-p CMOS logic give its advantages and disadvantages	Apply	6
10	**Explain** basic circuit concepts such as RS, area capacitances.	Apply	6
11	**Derive** the expression for time delay Ts_d in case of MOSFET	Apply	6
12	**Discuss** the issues involved in driving large capacitive loads in VLSI circuit regions.	Understand	6
13	**Describe** three sources of wiring capacitances. Discuss the wiring capacitance on the performance of a VLSI circuit	Understand	6
14	**List** the logical constraints of layers	Remember	6
	UNIT – V		
1	**Explain** description for half adder and Full adder.	Understand	7
2	**Draw** the logic diagram of zero/one detector and explain its operation with the help of stick diagram.	Apply	7
3	**Draw** the schematic and explain the principle and operation of Array Multiplier.	Apply	7
4	**Explain** the carry look ahead Adder	Understand	7
5	**Explain** the design hierarchies and bring out which kind of approach is better to adopt for system design.	Apply	7
6	**Describe** briefly n-bit parallel adder.	Apply	7
7	**Draw** and explain the structure barrel shifter.	Remember	7
8	**Discuss** the circuit design considerations in case of static adder circuits	Remember	7
9	**How** Boolean functions are performed using MUX. Discuss 1-bit CMOS implementation of ALU	Apply	7
10	**Sketch** the schematic serial parallel multiplier and explain its operation	Apply	7
11	**Discuss** synchronous and asynchronous counters	Remember	7
	UNIT – VI		
1	**Discuss** in detail about classification of memory arrays.	Understand	8
2	**Explain** the memory cell read and write operation of 6T SRAM with neat sketches.	Understand	8
3	**Explain** the principles of SRAM and DRAM.	Understand	8
4	**What** are the advantages of SRAM and DRAMs compare them in all respects.	Remember	8
5	**Explain** the read and write operations of 1T DRAM memory cell	Remember	8
6	**Explain** the read and write operations of 3T DRAM memory cell	Remember	8
7	**Explain** about NAND based ROM design.	Remember	8
8	**Explain** about NOR based ROM design.	Remember	8
9	**Discuss** about different types of ROMs	Remember	8
10	**Explain** various types of serial access memories with sketches.	Understand	8
11	**What** is content addressable memory and give any one application of it.	Understand	8
	UNIT – VII		
1	**Discuss** the different methods of programming of PALs	Understand	9
2	**Distinguish** PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects.	Remember	9
3	**Explain** about the principle and operation of FPGAs. What are its applications?	Understand	9

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
4	**Draw** the schematic for PLA and explain the principle. What are the advantages of PLAs?	Apply	9
5	**Explain** the structure and principle of PLA.	Understand	9
6	**Draw** the schematic and examine how Full Adder can be implemented using PLA's.	Apply	9
7	**Explain** about configurable FPGA based I/O blocks.	Understand	9
8	**Design** JK Flip flop circuit using PLA.	Apply	9
9	**Explain** semicustom design approach of an IC	Understand	9
10	**Compare** semicustom and full custom designs of an IC	Remember	9
	UNIT – VIII		
1	**Explain** the various DFT techniques.	Understand	10
2	**Discuss** about signature analysis in Testing. Explain with an example.	Understand	10
3	**Explain** about memory-self test with the help of a schematic	Understand	10
4	**Analyze** the issues to be considered while implementing BIST and explain each.	Remember	10
5	**Explain** how layout design can be done for improving testability.	Remember	10
6	**Explain** about different fault models in VLSI testing with examples.	Remember	10
7	**Analyze** any TWO a) DFT b) BIST c) Boundary scan Testing	Remember	10
8	**Explain** fault models.	Understand	10
9	**Explain** ATPG.	Understand	10
10	**Briefly** explain a) Fault grading & fault b) simulation Delay fault testing c) Statistical fault analysis	Understand	10
11	**Discuss** scan-based test techniques.	Understand	10
12	**Explain** Ad-Hoc testing and chip level test techniques.	Remember	10
13	**Explain** self-test techniques.	Remember	10
14	**Explain** system-level test techniques	Remember	10
15	**Explain** a) BILBO b) TAP controller c) Observability d) Controllability	Understand	10

GROUP-III (ANALYTICAL QUESTIONS)

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
	UNIT – I		
1	**Explain** lithography process with sketches	Understand	1
2	**Explain** diffusion process in IC fabrication	Understand	1

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
3	**Discuss** the purpose of metallization in IC manufacturing? Explain the methods employed for metallization	Understand	1
4	**How** integrated passive components are fabricated in ICs? Explain	Understand	1
5	**Mention** the properties of oxidation. Explain about thermal oxidation process	Understand	1
6	**Explain** how a bipolar NPN transistor is included in n-well CMOS processing. Draw the cross section of BiCMOS transistor.	Understand	1
	UNIT – II		
1	Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm (λ = 25 nm). Let *W*/*L* = 4/2 λ (i.e., 0.1/0.05 µm). In this process, the gate oxide thickness is 10.5 A. **Estimate** the high-field mobility of electrons to be 80cm2/V· s at 70 ^{o} C. The threshold voltage is 0.3 V. Plot *Ids* vs. *Vds*for *Vgs*= 0, 0.2, 0.4, 0.6, 0.8, and 1.0 V using the long-channel model.	Apply	2
2	**Calculate** the diffusion parasitic $C_{db}$of the drain of a unit-sized contacted nMOS transistor in a 65 nm process when the drain is at 0 V and again at *VDD* = 1.0 V. Assume the substrate is grounded. The diffusion region conforms to the design rules from Figure 2.8 with λ = 25 nm. The transistor characteristics are *CJ* = 1.2 fF/µm^2, *MJ* = 0.33, *CJSW* = 0.1 fF/µm, *CJSWG* = 0.36 fF/µm, *MJSW* = *MJSWG* = 0.10, and 0 = 0.7 V at room temperature.	Apply	2
3	Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8 × 1017 cm–3. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?	Apply	2
4	**What** is the minimum threshold voltage for which the leakage current through an OFF transistor (V_{gs}= 0) is 10^3 times less than that of a transistor that is barely ON (V_{gs}= V_t) at room temperature if *n* = 1.5. One of the advantages of silicon-on insulator (SOI) processes is that they have smaller *n*. What threshold is required for SOI if *n* = 1.3.	Apply	2
5	**Consider** an nMOS transistor in a 0.6 µm process with *W*/*L* = 4/2 λ (i.e., 1.2/0.6 µm). In this process, the gate oxide thickness is 100 A and the mobility of electrons is 350 cm^2/V· s. The threshold voltage is 0.7 V. Plot I_{ds}vs. $V_{ds}$for V_{gs}= 0, 1, 2, 3, 4, and 5 V.	Apply	2
6	**Derive** an equation for I_{dc} of an n channel process of twin well MOSFET operating in saturation region.	Apply	2
7	AN nMOS transistor is operating in saturation region with the following parameters. V_{gs}=5V, V_{th}=1.2V.(W/L)=10, µCox=110µ A/V_2. Find transconductance of the device.	Apply	2
8	For a CMOS inverter, **calculate** the shift in the transfer characteristic curve when βn/ βp ratio is varied from 1/1 to 10/1.	Apply	6
9	Find g_m and $r_{ds}$for an n-channel transistor with V_{gs}=1.2V,V_{th}=0.8V.(W/L)=10, µCox=92µ A/$V_2$and V_{DS} = V_{eff} +0.5V. The output impedance constant=0.0953V-^{1}.	Apply	6
10	**Draw** the pass transistor arrangement for the logic X=ABC.	Apply	6
	UNIT – III		
1	**Sketch** a stick diagram for a CMOS gate computing $Y = (A + B + C) \cdot D$ and estimate the cell width and height.	Apply	4
2	**Design** a layout diagram for the CMOS logic shown below $Y = ((A + B).C)$.	Apply	4

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
3	**Design** a stick diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$.	Apply	4
4	**Design** a stick diagram for two input pMOS NAND and NOR gates.	Apply	4
5	**Design** a stick diagram for the CMOS logic for $\overline{AB + CD}$	Apply	4
6	**Design** a layout diagram for the pMOS logic $Y = \overline{A(B + C)}$	Apply	4
7	**Design** a layout diagram for two input nMOS NAND gate.	Apply	4
8	**Design** a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	Apply	4
9	**Draw** the stick diagram and mask layout for a CMOS two input NOR gate.	Apply	4
	UNIT – IV		
1	**Calculate** the gate capacitance value of 5mm technology minimum size transistor with gate to channel capacitance value is 0.0004 $pF/mm^{2.}$	Apply	5
2	**What** is the problem of driving large capacitive loads? Explain a method to drive such load.	Understand	5
3	**Calculate** the rise time and fall time of the CMOS inverter (W/L)n=6 and (W/L)p=8. $k_n^{'} = 150\mu A / V^2$, $V_{tn} = 0.7V$, $k_p^{'} = 62\mu A / V_2$, $V_{tp} = -0.85V, V_{DD} = 3.3V.$ Total output capacitance =150Ff	Apply	5
4	**Realize** the function f=AB+CD using pseudo-nMOS logic.	Apply	5
5	**Realize** the function $f = \overline{A + BC}$	Apply	5
6	**Derive** the expression for rise and fall time of CMOS inverter. Comment on the expression derived.	Apply	5
7	**State** the problem that arises when comparatively large capacitive loads are driven by inverters. Explain how super buffers can solve the problem.	Apply	5
8	**Explain** 2:1 multiplexer using transmission gate and tristate inverter.	Apply	5
	UNIT – V		
1	**Draw** circuit diagram of one transistor with capacitor dynamic RAM and also draw its layout.	Apply	7
2	**Draw** the circuit diagram for 4X4 barrel sifter using complementary transmission gates and explain its shifting operation.	Apply	7
3	**Design** an incrementer circuit using counter.	Apply	7
4	**Design** ripple structure for one-zero detector circuit.	Apply	7
5	**Design** a comparator using XNOR gates.	Apply	7
6	**Design** sum and carry expressions of carry look ahead adder using nMOS logic.	Apply	7
7	**Design** a 4-bit array multiplier and implement using basic gates.	Apply	7
	UNIT – VII		
1	**Implement** JK flip-flop using PROM.	Apply	9
2	**Implement** 2-bit comparator using PAL logic.	Apply	9
3	**Draw** and explain the antifuse structure for programming the PAL device.	Apply	9
4	**Implement** $Y = \overline{A}.\overline{C} + AB + AC\overline{D}$ using programmable logic array (PLA).	Apply	9

S. No.	Questions	Bloom's Taxonomy Level	Course Outcome
5	**Implement** $Y = \overline{A}.\overline{C} + AB + AC\overline{D}$ using programmable array logic (PAL).	Apply	9
6	**Implement** $Y = \overline{A}.\overline{C} + AB + AC\overline{D}$ using programmable logic read only memory (PROM).	Apply	9
7	**Design** a 1-bit full adder and implement the sum and carry expressions using PLA.	Apply	9
	UNIT – VIII		
1	**Draw** the basic structure of parallel scan and explain how it reduces the long scan chains.	Understand	10
2	**Explain** how an improved layout can reduces faults in CMOS circuits	Understand	10
3	**Draw** the state diagram of TAP controller and explain how it provides the control signals for test data and instruction register.	Understand	10
4	A sequential circuit with n inputs and m storage devices. To test this circuit how many test vectors are required?	Apply	10
5	**How** IDDQ testing is used to test the bridge faults?	Understand	10
6	**What** is ATPG? Explain a method of generation of test vector.	Understand	10