Code No: R1632044 **R16** SET - 1

III B. Tech II Semester Regular/Supplementary Examinations, October/November - 2020

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A **(14 Marks)**

1. a) State properties of ROC. [2M]
b) Define DFT and IDFT. [2M]
c) How one can design digital filters from analog filters? [2M]
d) What are the advantages of the Kaiser window? [3M]
e) What do you mean by downsampling? [3M]
f) Explain about Multiple Access Memory. [2M]

PART –B **(56 Marks)**

2. a) Find the convolution of the signals $x(n)=(a)^n u(n)$ and $h(n)=(b)^n u(n)$. [7M]
b) Explain in detail the classification of discrete-time systems. [7M]

3. a) Compute the 8-point DFT of the sequence x(n)=1, $0\le n\le 7$ and x(n)=0, otherwise; by using DIT algorithms. [7M]
b) Find the inverse DFT of X(k) = {1,2,3,4}. [7M]

4. a) Describe various Structures of IIR filters. [7M]
b) Design a Chebyshev filter with a maximum passband attenuation of 2 dB; at Ω_p=20rad/sec and the stopband attenuation of 35 dB at Ω_s=50 rad/sec. [7M]

5. a) Explain the design of FIR filters using windows. [7M]
b) Given a 3-stage lattice FIR filter with coefficients, k_1=(1/4); k_2=(1/2); k_3=(1/3); Determine the FIR filter coefficients for the direct form structure. [7M]

6. a) Describes and derive sampling rate conversion by a rational factor I/D in multirate signal processing. [7M]
b) Consider a Sample sequence x[n]={0,1,2,3,6,9,10,12,15}. Draw the new signal using Linear Decimation and Interpolation by a factor L=3. [7M]

7. a) Explain in brief memory access schemes in DSP processors. [7M]
b) Briefly explain the following for TMS320C5X: [7M]
i) Flags available in status register ii) Parallel Logic Unit.

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