1. Which is interrupt-driven program?
a. getkey
b. inkey
c. sunkey
d. lcdkey

2. Which is interrupt-driven program?
a. getkey
b. codekey
c. sunkey
d. lcdkey

3. The routine ____ constant scans a 10-key pad via ports 0 and 3.
a. getkey
b. inker
c. codekey
d. bigkey

4. The program _____ uses both hardware timers, T0 and T1.
a. getkey
b. inker
c. codekey
d. bigkey

5. The program _____ is interrupt-driven by a high-to-low transition on INTD.
a. getkey
b. inker
c. codekey
d. bigkey

6. The ____ program can scan an 8 X 8 keyboard matrix using to generate a periodic 2ms delay in an interrupt mode.
a. getkey
b. inker
c. odekey
d. bigkey

7. The completely interrupt-driven small keyword example is
a. getkey
b. inker
c. codekey
d. bigkey

8. The ____ works best when handling data in byte-sized packages.
a. 8031
b. 8051
c. 8071
d. 8081

9. The ____ program canbe modified to use a timer to generate associated with the key-down de bounce time and the "all-up" delay.
a. getkey
b. inker
c. codekey
d. bigkey

10. A _____ keboard is interfaced with 8051 microcontroller.
a. 16-key
b. 32-key
c. 64-key
d. 128-key

11. _____ displays commonly contain LED segments arranged as an 8.
a. seven segment display
b. intelligent LCD display
c. 4X4 display
d. 2X2 display

12. The program ____ displays sharacters found in locations ch1 to ch4 on four common-cathode seven- segment displays.
a. svnseg
b. lcdisp
c. lcdisp2
d. svnseg3

13. In intelligent LCD display, D0 to D7 are located at
a. 1 to 7 pins
b. 7 to 14 pins
c. 2 to 8 pins
d. 8 to 16 pins

14. The ____ display contains two internal byte-wide registers.
a. seven segment display
b. intelligent LCD display
c. 4X4 display
d. 2X2 display

15. ____ displays include incandescent and, more likely, LED indicators.
a. single light
b. double light
c. single character
d. intelligent alphanumeric

16. _____ displays include numeric and alphanumeric arrays.
a. single light
b. dou7ble light
c. single character
d. intelligent alphanumeric

17. _____ displays are equipped with a built-in microcontroller.
a. single light
b. double light
c. single character
d. intelligent alphanumeric

18. The program ____ displays sharacters found in locations ch1 to ch4 on four common-cathode seven- segment displays.
a. svnseg
b. lcdisp
c. lcdisp2
d. svnseg3

19. The program _____ is very cumbersome when many messages must be displayed.
a. svnseg
b. lcdisp
c. lcdisp2
d. svnseg3

20. 20 characters per line display can be possible in
a. seven segment display
b. intelligent LCD display
c. 4X4 display
d. 2X2 display

21. Control sequence of D/A conversion is
a. CS then WR
b. WR then CS
c. CS then WR then RD
d. WR then RD
22. Control sequence of A/D conversion is
a. CS then WR
b. WR then CS
c. CS then WR then RD
d. WR then RD
23. A/D conversion time is
a. 1 μs
b. 2 μs
c. 3 μs
d. 4 μs
24. For a 1000-hertz wave, S could be _____ samples.
a. 50d
b. 100d
c. 150d
d. 200d
25. D/A conversion time is
a. 3 μs
b. 4 μs
c. 5 μs
d. 6 μs
26. The frequency of the counted pulse train is
a. unknown frequency = counter / timer
b. unknown frequency = counter X timer
c. unknown frequency = counter - timer
d. unknown frequency = counter + timer
27. If the counter counts 200 pulses over an interval of 0.1 second generated by the timer, the
frequency is
a. 200 Hz
b. 2000Hz
c. 20000Hz
d. 200000Hz
28. The frequency of the pulse value in D/A conversion is
a. UF = 1 / (wave time high X 2)
b. UF = 1 / (wave time high + 2)
c. UF = 1 / (wave time high - 2)
d. UF = 1 / (wave time high / 2)
29. Reference voltage value in D/A conversion is
a. ±8V
b. ±10V
c. ±12V
d. ±14V
30. A/D converters use _____ types.
a. SAR
b. flash
c. magnetic
d. bubble
31. A/D converters use _____ types.
a. SAR
b. flash
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b. lcdisp
c. lcdisp2
d. svnseg3
34. The ___ display contains two internal byte-wide registers.
a. seven segment display
b. intelligent LCD display
c. 4X4 display
d. 2X2 display
35. The 8051 external input pin is
a. INT1
b. DPH
c. DPL
d. IE
36. The 8051 external input pin is
a. INT0
b. DPH
c. DPL
d. IE
37. Reference voltage value in D/A conversion is a) b) c) d)
a. ±8V
b. ±10V
c. ±12V
d. ±14V
38. A/D conversion time is
a. 1 μs
b. 2 μs
c. 3 μs
d. 4 μs
39. In intelligent LCD display, D0 to D7 are located at
a. 1 to 7 pins
b. 7 to 14 pins
c. 2 to 8 pins
d. 8 to 16 pins
40. _____ displays commonly contain LED segments arranged as an 8.
a. seven segment display
b. intelligent LCD display
c. 4X4 display
d. 2X2 display
41. ____ is not suitable for the interchange of data between 8051 microcontrollers.
a. mode 0
b. mode 1
c. mode 4
d. mode 3
42. Data transmission using modes 2 and 3 features ___ bits per character.
a. 8
b. 9
c. 10

d. 11

43. Which serial data communication mode is multiprocessor 9-bit UART?
a. mode 0
b. mode 1
c. mode 2
d. mode 4

44. Which serial data communication mode is standard 8-bit UART?
a. mode 0
b. mode 1
c. mode 4
d. mode 3

45. Which is used for time-sharing applications?
a. Star
b. loop
c. hybrid
d. bus

46. Which is used for data-gathering applications?
a. Star
b. loop
c. hybrid
d. bus

47. The ___ is a good choice when the number of nodes is small.
a. Star
b. loop
c. hybrid
d. bus

48. Which serial data communication mode is standard 8-bit UART?
a. mode 0
b. mode 1
c. mode 2
d. mode 3

49. Which serial data communication mode is high speed?
a. mode 0
b. mode 1
c. mode 2
d. mode 3

50. Which serial data communication mode is 8-bit shift register?
a. mode 0
b. mode 1
c. mode 2
d. mode 3

51. A standard for OS interfaces proposed by IEEE is
a. POSIX
b. QNX
c. AMX
d. Intel

52. The basic building block of software written under an RTOS is the
a. scheduler
b. task
c. context
d. reentrancy

53. The ___ state means that this task has not got any thing to do right now, even if the microprocessor become available.
a. running
b. ready
c. blocked
d. suspended

54. A _____ function may not use the hardware in a nonatomic way.
a. mutex
b. task
c. reentrant
d. semaphore

55. Under most RTOS a task is simply a _____.
a. routine
b. subroutine
c. interrupt
d. exception

56. A ____ RTOS will stop a lower-priority task as soon as the higher-priority task unblocks.
a. preemptive
b. non preemptive
c. interpret
d. exception

57. A_____ RTOS will only take the microprocessor away from the lower-priority task when that task blocks.
a. preemptive
b. non preemptive
c. interpret
d. exception

58. A function that works properly even if it is called by more than one task is called a ____ function.
a. mutex
b. task
c. reentrant
d. semaphore

59. The ____ state means that the microprocessor is executing the instructions that make up this.
a. running
b. ready
c. blocked
d. suspended

60. The ___ state means that some other task is in the running state but that this task ha things that it could do if the microprocessor becomes available.
a. running
b. ready
c. blocked
d. suspended

61. A semaphore that does not specify the order in which processes are removed from the queue is _____
a. mutex
b. strong
c. counting

d. weak

62. The process that has been blocked the longest is released from the queue hint:
a. mutex
b. strong
c. counting
d. weak

63. semaphores [c]
a. are used to do I/O
b. synchronize critical resources to present condition.
c. synchronize critical resources to present dead lock.
d. allow processes to communicate with one another.

64. The non-binary semaphore is often referred to as _____ semaphore
a. mutex
b. strong
c. counting
d. weak

65. Binary semaphore is also known as
a. General semaphore
b. Mutex
c. Cluster
d. Spooling

66. For both counting semaphores and binary semaphores, a _____ is used to hold processes
waiting on the semaphores.
a. stack
b. queue
c. dequeue
d. circular queue

67. _____ guarantee freedom from starvation.
a. Strong semaphores
b. Weak semaphores
c. Delay semaphores
d. Binary semaphores

68. The barbershop problem is an example of
a. Deadlock
b. Starvation
c. Semaphore
d. Live lock

69. In the producer/consumer problem, there are
a. one or more producers and one or more consumers
b. single producer and single consumer
c. single producer and one or more consumers
d. one or more producers and single consumer

70. A semaphore count of negative n means (s= -n) that the queue contains waiting process. [b]
a. n+1
b. n
c. n-1
d. 0

71. _____ can be considered as an array of mailboxes
a. pipes
b. semaphore
c. timer
d. message queue

72. In a time sharing operating system, when the time slot given to a process is completed , the
process goes from the RUNNING state of the
a. BLOCKED state
b. READY state
c. SUSPENDED state
d. TERMINATE state

73. a mutex can be
a. locked state
b. unlocked state
c. either in locked state or unlocked state
d. neither in locked state nor unlocked state

74. A task owning a mutex, can not be _____
a. added
b. modified
c. released
d. deleted

75. Array of mailboxes can be considered as
a. pipes
b. semaphore
c. timer
d. message queue

76. Mutex stands for
a. mutual text
b. mutual exclusion
c. mutual task
d. mutual timer

77. _____ occurs when two or more tasks wait for a resource being held by another task
a. deadlock
b. live lock
c. semaphore
d. starvation

78. Mutual exclusion problem occurs between
a. two disjoin process that do not interact
b. processes that share resources
c. processes that do not use the same resource
d. processes have priority

79. What problem is solved by dijkstra s bankers algoritham?
a. mutual exclusion
b. deadlock recovery
c. deadlock avoidance
d. cache coherence

80. Mutex is a special
a. count semaphore
b. binary semaphore
c. task semaphore
d. time semaphore

81. A common use of ____ is to serve as the program memory for a micro processor
a. ROM
b. EPROM
c. EEPROM
d. Flash memory

82. to obtain better memory utilization dynamic loading ids used with dynamic loading a routine
is not loaded until it is called for implementing dynamic loading
a. special support from hardware is essential
b. special support from operating system is essential

c. special support from both hardware and operating system are essential

d. **user programs can implement dynamic loading without any special support from the**
operating system or the hardware

83. One common use of a _____ timer is to enable an embedded system to restart itself in case
of a failure
a. **watchdog**
b. special
c. reaction
d. proactive

84. _____ is an extension of EEPROM
a. RAM
b. SRAM
c. **Flash memory**
d. DRAM

85. _____ is really more of a bus interface architecture the DRAM architecture
a. EDORAM
b. **Rambus DRAM**
c. SDRAM
d. FPMDRAM

86. _____ are used to measure the elapsed time of events
a. **timers**
b. counters
c. schedulers
d. processes

87. A _____ is an extremely common peripheral devises that can measure time intervals
a. counters
b. **timers**
c. schedulers
d. process

88. To use a _____ , we must configure its inputs and monitors its outputs
a. counters
b. **timers**
c. schedulers
d. process

89. A _____ timer is an application that measures the time a person takes to respond to a
visual or audio stimulus
a. watchdog
b. special
c. **reaction**
d. proactive

90. System's _____ interrupt response time has to be considered while evaluating the
performance of an operating system embedded software
a. best-case
b. **worst-case**
c. average-case
d. all cases

91. ISR stands for
a. Interface service routine
b. Interrupt Service Runner
c. **Interrupt Service Routine**

d. Interface Standard Routine

92. When a process makes a system call, its mode change from
a. **user to kernel**
b. kernel to user
c. restricted to process
d. unrestricted to restricted

93. The technique that allows only one user to work with a file at a particular time is called
a. semaphore
b. critical region
c. **locking**
d. dedicated mode

94. _____ is a hardware signal that informs the CPU that an important event has occurred
a. event
b. signal
c. process
d. **interrupt**

95. When interrupt occurs , CPU saves its context and jumps to the _____
a. **ISR**
b. API
c. IP
d. ITS

96. The maximum time for which interrupts are disables + time to start the execution of the first
instruction in the ISR is called_____
a. Interrupt response time
b. Interrupt recovery time
c. **Interrupt latency**
d. Interrupt handler

97. Time between receipt of interrupt signal and starting the code that handles the interrupt is
called_____
a. **Interrupt response time**
b. Interrupt recovery time
c. Interrupt latency
d. Interrupt handler

98. Time required for CPU to return to the interrupted code/ highest priority task is called
a. Interrupt response time
b. **Interrupt recovery time**
c. Interrupt latency
d. Interrupt handler

99. In a preemptive kernel , response time =
a. Interrupt recovery time + time to save CPU registers context
b. Interrupt respond time + time to save CPU registers context
c. Interrupt handler + time to save CPU registers context
d. **Interrupt latency + time to save CPU registers context**

100. Principle of RTOS is
a. **write short interrupt routines**
b. you do not need tasks for priority
c. you need tasks for inheritance
d. consider turning time-slicing off

101. _____ causes more task switched and therefore cuts throughput.
a. time-slicing

b. encapsulation
c. priority
d. routines

102. Principle of RTOS is
a. write short interrupt routines
b. you do not need tasks for priority
c. you need tasks for inheritance
d. consider turning time-slicing on

103. Principle of RTOS is
a. write short interrupt routines
b. you need tasks for priority
c. you need tasks for inheritance
d. consider turning time-slicing on

104. Principle of RTOS is
a. write short interrupt routines
b. you do not need tasks for priority
c. you need tasks for encapsulation

d. consider turning time-slicing on

105. _____ determines if frame is addressed to telegraph.
a. DTP protocol task
b. ADSP protocol task
c. serial port task
d. Interrupt routine

106. _____ determines if frame is print data, status request, etc.
a. DTP protocol task
b. ADSP protocol task
c. serial port task
d. Interrupt routine

107. _____ determines if serial data contains new status.
a. DTP protocol task
b. ADSP protocol task
c. serial port task
d. Interrupt routine

108. _____ receives network frame or serial data.
a. DTP protocol task
b. ADSP protocol task
c. serial port task
d. Interrupt routine

109. The _____ stores the status and uses it when responding to later status request from the network.
a. DTP protocol task
b. ADSP protocol task
c. serial port task
d. Interrupt routine

110. For both counting semaphore and binary semaphore a ___ is used to hold processing waiting on the semaphores
a. stack
b. queue
c. dequeue
d. circular queue

111. the barber problem is an example of
a. dead lock
b. starvation
c. semaphore
d. live lock

112. Binary semaphore will take the values of _____
a. 0
b. 1
c. Either 0 or 1
d. Neither 0 nor 1

113. To access a shared resource , there should be a mechanism so that there is discipline . this is known as ____ synchronization
a. resource
b. task
c. shared
d. write

114. Binary semaphore is also known as
a. general semaphore
b. mutex
c. cluster
d. spooling

115. counting semaphore will have an integer value greater than _____
a. 0
b. 1
c. 2
d. 3

116. If an 8 bit integer is used for implementing a counting a semaphore , the semaphore can take a value between ___ and _____
a. 0 and 255
b. 0 and 65,535
c. 0 and 127
d. 0 and 63

117. In order to allow only one process to enter its critical section binary semaphore are initialized to
a. 0
b. 1
c. 2
d. 3

118. What is the initial value of the semaphore to allow only one of the many process to enter their critical section
a. 0
b. 1
c. 2
d. 3

119. Semaphore are used to solve the problem of
a. rare condition
b. process asynchronization
c. mutual exclusion
d. compilation

120. A _____ mechanism is used to get your software into your target for debugging purposes.
a. shared memory
b. virtual memory
c. secondary memory
d. overlay memory

121. A program that resides in the target ROM is

a. loader
b. compiler
c. monitor
d. linker
122. You should encapsulate semaphores, queues, and so on, in _____ modules so that the input between modules is a function call.
a. 3
b. 2
c. 1
d. 4
123. A device that replaces the ROM in the target system is
a. PROM
b. ROM emulators
c. In-circuit emulator
d. flash
124. A common feature of in-circuit emulator is
a. shared memory
b. virtual memory
c. secondary memory
d. overlay memory
125. A _____ understands the same C language as a native compiler.
a. cross-compiler
b. cross-assembler
c. linker/loader
d. re-compiler
126. A _____ understands as assembly language that is specific to your target microprocessor.
a. cross-compiler
b. cross-assembler
c. linker/loader
d. re-compiler
127. A _____ combines separately compiled and assembly modules into an executable image.
a. cross-compiler
b. cross-assembler
c. linker/loader
d. re-compiler
128. Linker/locators use _____ to decide where to put different parts of the code and data.
a. cross-compiler
b. cross-assembler
c. tool design
d. segments
129. One way to save data space in an embedded system that uses an RTOS is to make your tasks _____ only as large as they need to be.
a. stacks
b. queue
c. lists
d. records
130. _____ captures data without reference to any events on the circuit it is examining.
a. self-collected

b. clock
c. other hardware
d. monitors
131. The goal of typical testing process is
a. find the bugs lately
b. exercise all code
c. develop reusable, repeatable tests
d. keep audit trail of test
132. _____ use a combination of software and hardware to give you standard debugging capabilities.
a. self-collected
b. clock
c. state mode
d. monitors
133. RISC stands for
a. Reduced Instruction Set Computer
b. Reverse Instruction Set Computer
c. Run Instruction Set Computer
d. Range Instruction Set Computer
134. A _____ can capture one-time events.
a. oscilloscope
b. multimeter
c. storage scope
d. ohm meter
135. The goal of typical testing process is
a. find the bugs lately
b. exercise some code
c. develop reusable, repeatable tests
d. keep audit trail of test
136. Simulator disadvantage is
a. testing assembly-language code
b. resolving probability issues
c. shared-data bugs
d. determine response and through put
137. An oscilloscope is
a. analog device
b. digital device
c. converter
d. detector
138. _____ captures data without reference to any events on the circuit it is examining.
a. self-collected
b. clock
c. state mode
d. monitors
139. In _____ a logic analyzer can capture traces.
a. self-collected
b. clock
c. state mode
d. monitors
140. For both counting semaphores and binary semaphores, a _____ is used to hold processes waiting on the semaphores.
a. stack
b. queue
c. dequeue
d. circular queue

141. _____ guarantees freedom from starvation.
a. Strong semaphores
b. Weak semaphores
c. Delay semaphores
d. Binary semaphores

142. _____ is used for measuring resistance.
a. oscilloscope
b. emulator
c. ohm meter
d. multimeter

143. Voltmeter is used for
a. clock differences
b. voltage differences
c. resistance differences
d. Delay differences

144. Binary semaphore is also known as
a. General semaphore
b. Mutex
c. Cluster
d. Spooling

145. BDM stands for
a. Background Debug Monitor
b. Backend Debug Monitor
c. Based Debug Monitor
d. Bound Debug Monitor

146. ICE stands for
a. In-Circuit Emulator
b. In-Circuit Entrance
c. Extractor In-Circuit
d. In-Circuit Enabled

147. Merit of simulator is
a. shared-data bugs
b. other hardware
c. solving portability issues
d. testing assembly language code

148. _____ will work with any microprocessor.
a. emulators
b. logic analyzers
c. oscilloscope
d. monitors

149. Analog device is
a. oscilloscope
b. emulator
c. ohm meter
d. multimeter

150. "Overflow" condition code in ARM is
a. VC
b. VS
c. EQ
d. EZ

151. "Equals zero" condition code in ARM is
a. VC
b. VS
c. EQ
d. EZ

152. In _____, the value stored in the register is used as the address to be fetched from memory.
a. Register-indirect addressing
b. Direct addressing
c. Indirect addressing
d. Register-direct addressing

153. In _____, the value stored in the register is used as the address to be fetched from memory.
a. Register-indirect addressing
b. Direct addressing
c. Indirect addressing
d. Register-direct addressing

154. ARM has _____ general-purpose registers.
a. 6
b. 8
c. 12
d. 16

155. The _____ instruction is the basic mechanism is ARM for changing the flow of control.
a. A
b. B
c. C
d. D

156. ARM is actually a family of _____ architectures.
a. RISC
b. CISC
c. RISK
d. CISK

157. The standard ARM word is _____ bits length.
a. 8
b. 16
c. 32
d. 64

158. ARM comparison instruction is
a. MOV
b. MVN
c. LDR
d. TST

159. ARM comparison instruction is
a. MOV
b. MVN
c. LDR
d. TEQ

160. ARM load-store instruction is
a. CMP
b. MOV
c. CMN
d. ADR

161. The _____ operation is used for iterative algorithms.
a. MODE1
b. RECIPS
c. STKY
d. SCALB

162. The routing models used for floating-point arithmetic are controlled by two bits in the ___region.
a. MODE1
b. MODE2
c. STKY

d. SCALB

163. The SHARC ___ instruction provides procedure calls. a)
b) c) d)
a. JUMP
b. CALL
c. SEND
d. PROC

164. The _____ bits are set along with the ASTAT register
bits, but are not cleared.
a. MODE1
b. MODE2
c. STKY
d. SCALB

165. The _____ operation adds an integer value to the
exponent of a floating-point
operand.
a. MODE1
b. MODE2
c. STKY
d. SCALB

166. A SHARC instruction consists of _____ bits
a. 32
b. 48
c. 16
d. 8

167. The SHARC member is internally organized as _____
bit works.
a. 32
b. 48
c. 16
d. 8

168. The SHARC has _____ data address generators.
a. 5
b. 4
c. 3
d. 2

169. The _____ instruction is the basic mechanism for
changing the flow of control in the
SHARC.
a. JNZ
b. JMP
c. JUMP
d. JNN

170. What does the SHARC CLIP instruction do?
a. sets range
b. finds maximum
c. absolute value
d. compare

171. The address _____ is reserved for the extended 10-bit
addressing scheme in I2C.
a. 11100XX
b. 11111XX
c. 11110XX
d. 11000XX

172. The _____ bus has been used to support many I/O cards
for PC-based embedded
systems.
a. I2C

b. PCI
c. ISA
d. VME

173. SDL stands for
a. Serial discrete line
b. serial deliver line
c. serial divide line
d. serial data line

174. _____ encourages a data-push programming style.
a. I2C
b. CAT
c. LON
d. DSP

175. The address _____ is used to signal a general call in I2C.
a. 00000
b. 0000000
c. 0000
d. 000

176. The _____ bus is used in microcontroller-based systems.
a. I2C
b. CAN
c. LON
d. DSP

177. The _____ bus is a well-known as commonly used to link
microcontrollers in to
systems.
a. I2C
b. CAN
c. LON
d. DSP

178. The _____ bus is designed as a multimaster bus.
a. I2C
b. Can
c. LON
d. DSP

179. Which is used for the command interface in an MPEG-2
video chip.
a. I2C
b. Can
c. LON
d. DSP

180. SCL stands for
a. Serial Command Line
b. Series Clock Line
c. Serial Clock Line
d. Send Clock Line

181. CRC field length in the CAN bus is _____ bits.
a. 13
b. 14
c. 15
d. 16

182. Data field length in the CAN bus is ___ bits.
a. 0-28
b. 0-16
c. 0-64
d. 0-128

183. _____ is a synchronous bus.
a. I2C

b. CAN
c. Echelon LON
d. DSP

184. CRC stands for
a. Cyclic Removal Code
b. Cyclic Remote Code
c. Cyclic Redundancy Code
d. Cyclic Ready Code

185. An arbitration field in the CAN bus is ___ bits.
a. 13
b. 14
c. 15
d. 12

186. CAN bus stand for
a. Controller Area Network
b. Converter Area Network
c. Connection Area Network
d. Coded Area Network

187. The ____ bus was developed for automotive electronics.
a. I2C
b. CAN
c. LON
d. DSP

188. The ____ network was developed for home and industrial automation.
a. I2C
b. CAN
c. Echelon LON
d. DSP

189. The _____ bus uses bit-serial transmission.
a. I2C
b. CAN
c. Echelon LON
d. DSP

190. Control of the _____bus is arbitrated using CSMA/AMP.
a. I2C
b. CAN
c. Echelon LON
d. DSP

191. _____ is used for network management services.
a. TCP
b. IP
c. HTTP
d. UDP

192. TCP stands for
a. Transmission Condition Protocol
b. Transmission Control Protocol
c. Transmission Cancel Protocol
d. Transmission Cooperative Protocol

193. The simplest way to test the controllers to build an elevator simulator using an _____ .
a. APGA
b. CPGA
c. EPGA
d. FPGA

194. The IP address is typically written in the form

a. XXX.XX.XX.XX
b. XXX.XX.XX.XXX
c. XX.XX.XX.XX
d. XX.X.XX.XX

195. _____ creates packets for routing to the destination.
a. TCP
b. IP
c. HTTP
d. SMTP

196. A node that transmits data among different types of networks is known as a _____ .
a. router
b. linker
c. receiver
d. layer

197. DNS stands for
a. Domain Name Source
b. Domain Name Server
c. Domain Name Service
d. Domain Name Sender

198. Using IP as the foundation, TCP is used to provide ____ for batch file transfers.
a. HTTP
b. SMTP
c. FTP
d. SNMP

199. Using IP as the foundation, TCP is used to provide _____ for World Wide Web service.
a. HTTP
b. SMTP
c. FTP
d. SNMP

200. Using IP as the foundation, TCP is used to provide _____ for email.
a. HTTP
b. SMTP
c. FTP
d. SNMP