

II B. Tech I Semester Supplementary Examinations, May - 2019
SWITCHING THEORY AND LOGIC DESIGN
 (Com to ECE, EIE and ECC)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answer **ALL** the question in **Part-A**
 3. Answer any **FOUR** Questions from **Part-B**

PART -A

1. a) Convert the given gray code number to binary: 1001001011. (2M)
- b) Prove that $Y=AB + BC + AC$ is a self-dual function. (3M)
- c) Draw four bit adder circuit using full adders (3M)
- d) Explain difference in the basic structure of PLA, PAL and PROM (2M)
- e) Convert D Flip Flop to T Flip Flop (2M)
- f) Explain about Mealy state machine (2M)

PART -B

2. a) Realize a 2 input EX-OR gate using minimum number of 2 input NAND gates. (7M)
- b) Encode the decimal numbers using 6, 3, 1,-1 weighted code. Is it a self-complementing code? (7M)
3. a) Simplify the Boolean function F using the don't care conditions d, in (i) sum of products and (ii) product of sums. (7M)

$$F= A'B'D' + A'CD+A'BC$$

$$d=A'BC'D+ACD+AB'D'$$
- b) $F(A, B, C, D) = \pi \max [5, 8, 14] + d\pi [7, 11, 12, 13, 15]$. Obtain minimal sop (7M) function.
4. a) Define Multiplexer and explain the procedure to implement 32X1 MUX by Using 4X1 Multiplexers. (7M)
- b) Design 4-bit digital comparator and explain with neat sketch. (7M)
5. a) Write a brief note on Architecture of PLDs (7M)
- b) Write a brief note on Capabilities and the limitations of threshold gates. (7M)
6. a) Draw the circuit diagram of MOD-10 Counter and explain the operation of it. (7M)
- b) What is race around condition and how to avoid it along with circuit diagram. (7M)



Code No: R1621042

R16**SET - 1**

7. a) Distinguish between Mealy and Moore machines (7M)
b) Convert the following Mealy machine into a corresponding Moore machine: (7M)

PS	NS,Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

